



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/271,691  
Filed: March 18, 1999  
Inventor(s):  
Craig M. Conway

Examiner: Vincent, David Robert  
Group/Art Unit: 2661  
Atty. Dkt. No: 5150-30300

#11M

Title: System and Method for  
Efficiently Generating Packets on  
a Serial Bus in  
Response to Parallel Bus Cycles

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Jeffrey C. Hood

Signature: JCH Date: 3/19/2003

SUBMISSION OF FORMAL DRAWINGS

Official Draftsman  
Commissioner for Patents  
Washington, D.C. 20231

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Technology Center 2600

Sir:

Applicant hereby submits the formal drawings for the above-referenced application and requests that these drawings (Figures 1-11C on 10 sheets) be accepted for filing.

Respectfully submitted,

JCH

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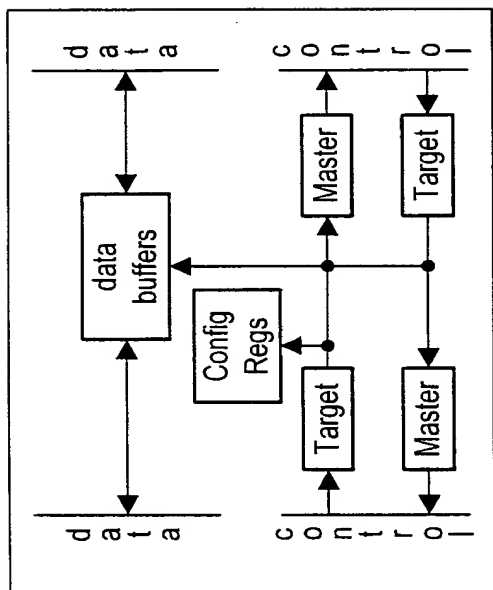


FIG. 1  
 PCI-PCI Bridge Block Diagram

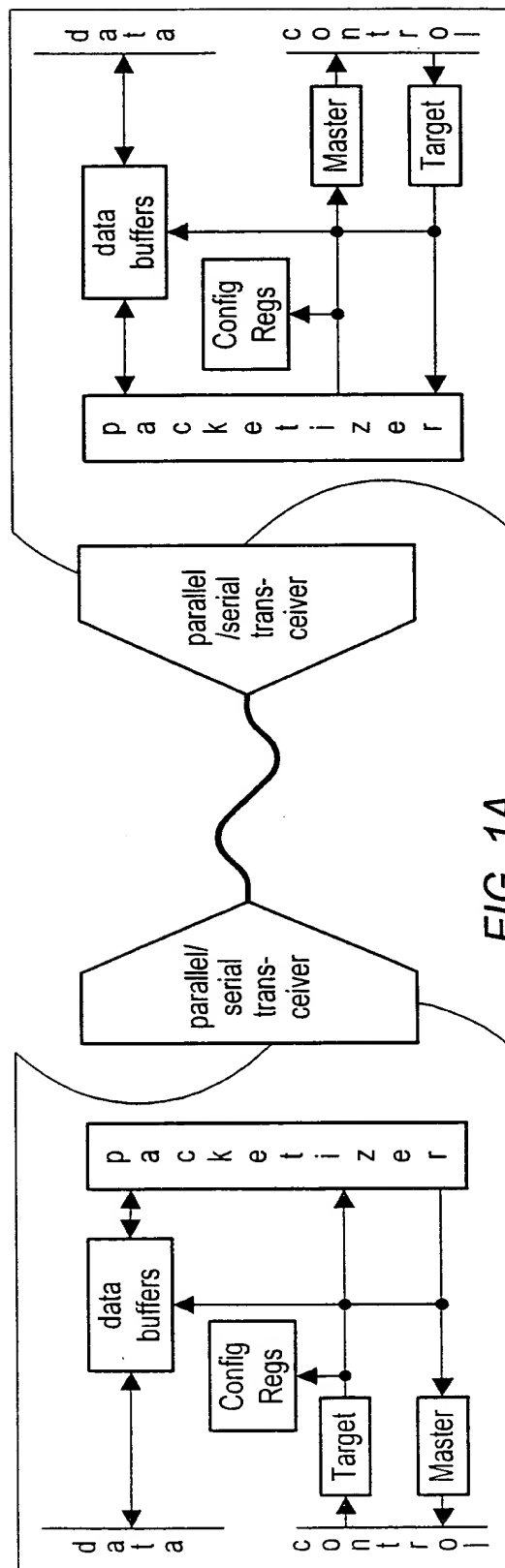
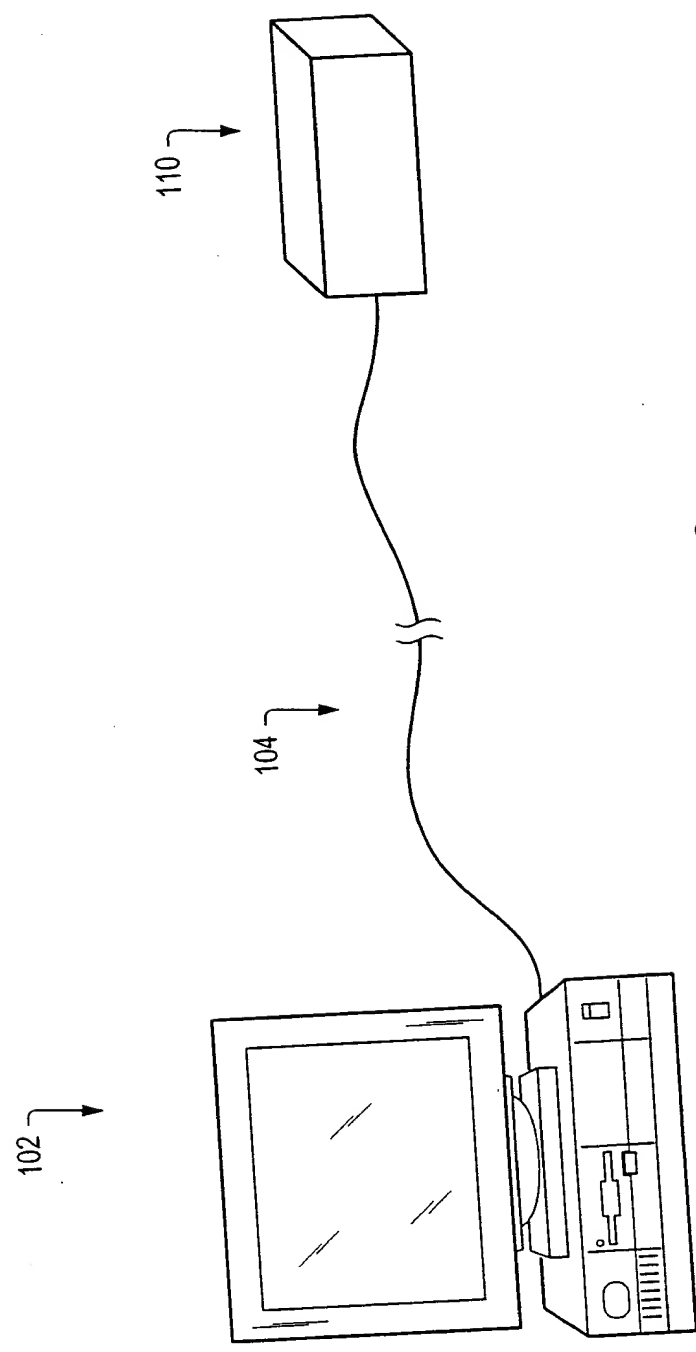


FIG. 1A  
 Block System Diagram

APPROVED	O.G. FIG.
CLASS	SUBCLASS

PBE JC66  
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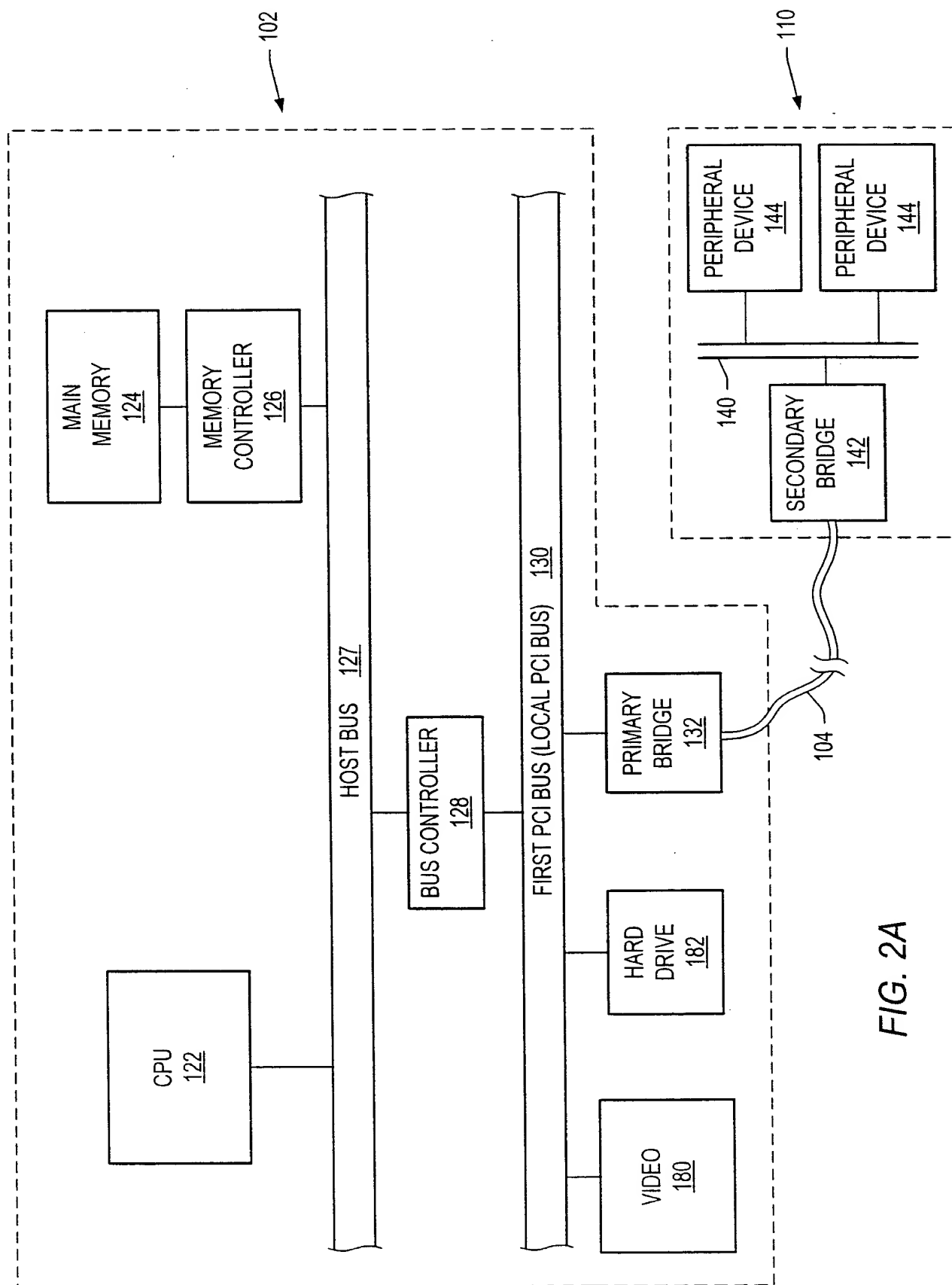
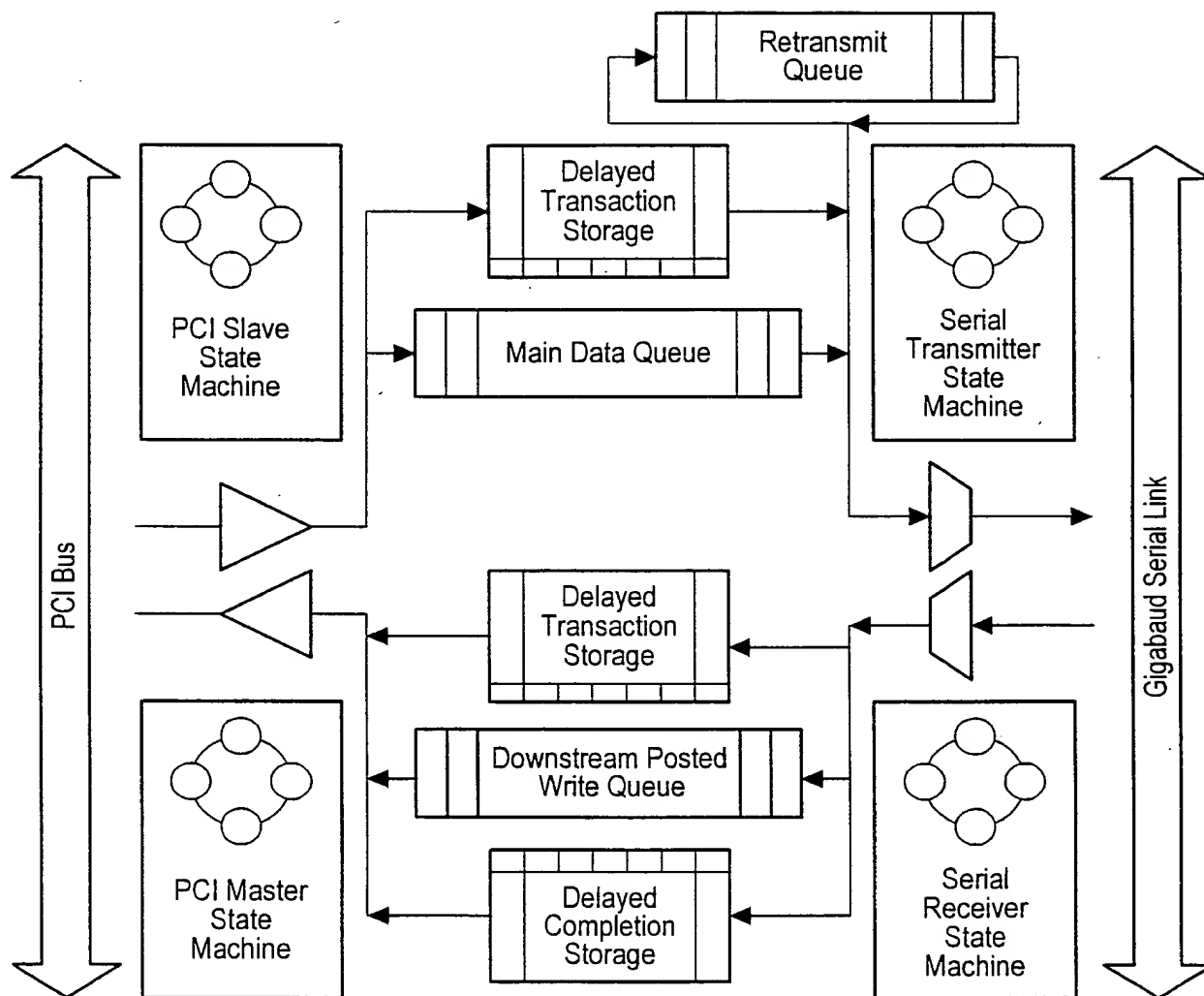
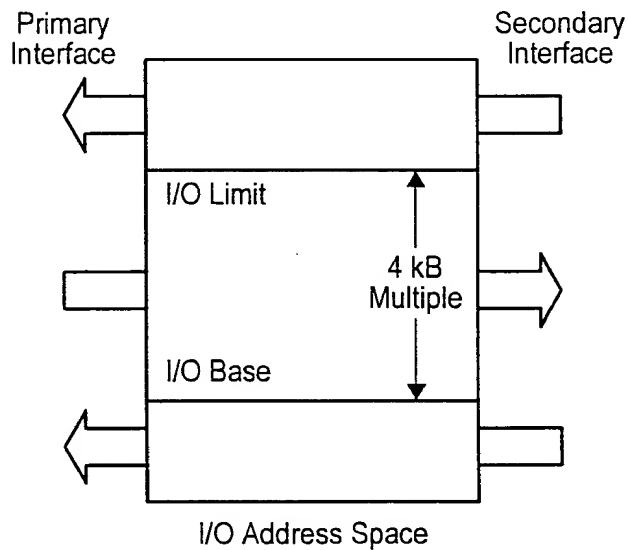


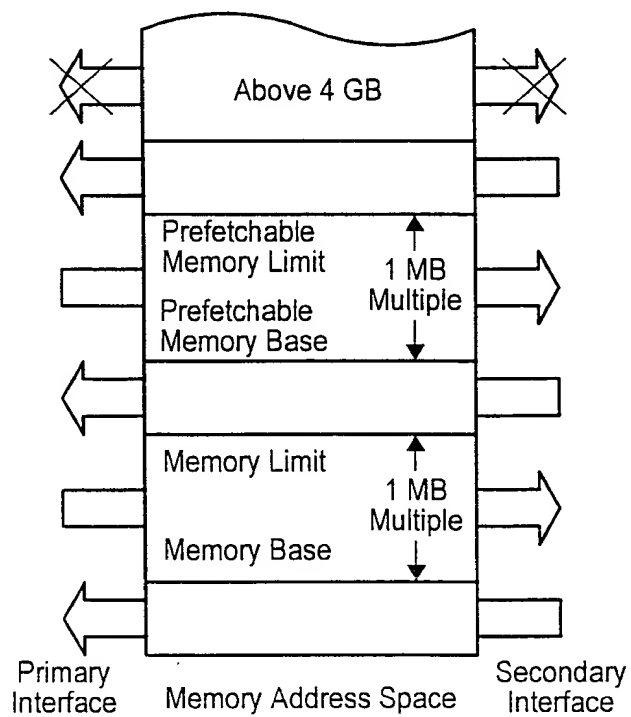
FIG. 2A



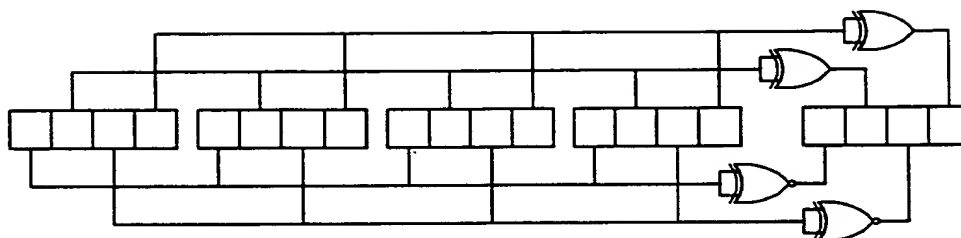
**FIG. 3**  
*WASP Block Diagram*



**FIG. 4**  
*I/O Transaction Forwarding Map*



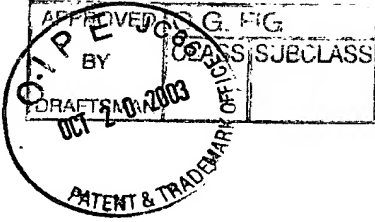
**FIG. 5**  
*Memory Transaction Forwarding Map*



**FIG. 6**  
*WASP Frame Format and Parity Generation*

Description		17	16	15 12	11 8	7 4	3 0
Posted Write	PW	U	ParErr	1000	PCI Cmd	PCI BE	Par
PCI Configuration	PCR	U	ParErr	1001	PCI Cmd	PCI BE	Par
Delayed Request 0	DR0	U	ParErr	1100	PCI Cmd	PCI BE	Par
Delayed Request 1	DR1	U	ParErr	1101	PCI Cmd	PCI BE	Par
Delayed Request 2	DR2	U	ParErr	1110	PCI Cmd	PCI BE	Par
Delayed Completion	DC	U	ParErr	1111	PCI Cmd	PCI BE	Par
Success Ack	SA	U	U	0001	U	U	Par
Failure Ack	FA	U	U	0010	U	U	Par
Sanity Check	SC	U	U	0011	U	U	Par
Reset	RST	U	U	0100	U	U	Par
Power On	POP	U	U	0101	U	U	Par

**FIG. 7**  
*Command Packets*



Error Condition	Response
Bad PAR on title frame of command packet	ignore transfer
Bad PAR on packet count frame of command packet	submit Failure ACK if received packet is not a Failure ACK or a Sanity Check
Bad PAR on data packet	submit Failure ACK
Receipt of data packet after fill frame (i.e. command packet did not start transfer)	ignore rest of transfer
Received packet count does not match packet counter	submit Failure ACK

FIG. 8  
Error Condition Responses

Bits 33:32	Bits 31:0
00	Command Frame
01	PCI Address Frame or Regular Data Frame
10	PCI Data Frame
11	Reserved

FIG. 9  
RTQ Packet Encoding

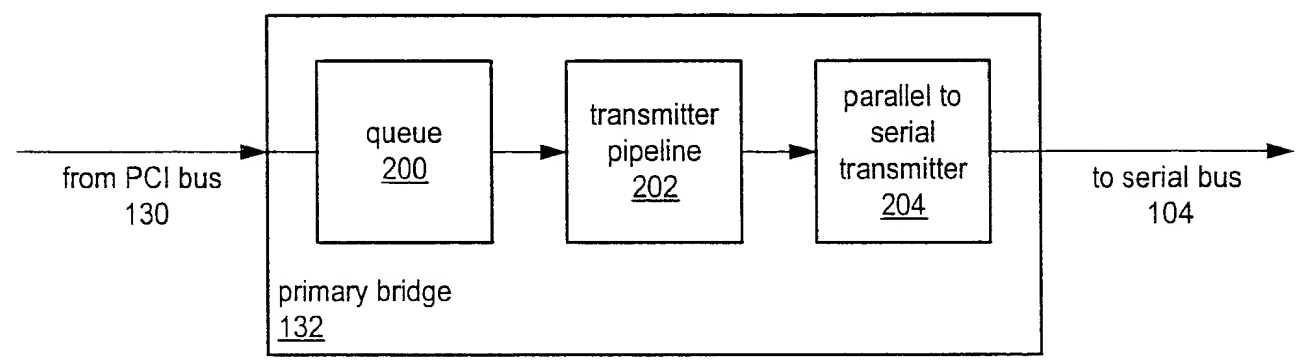
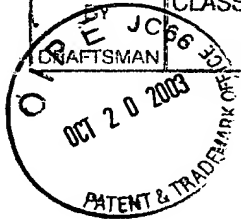


FIG. 10





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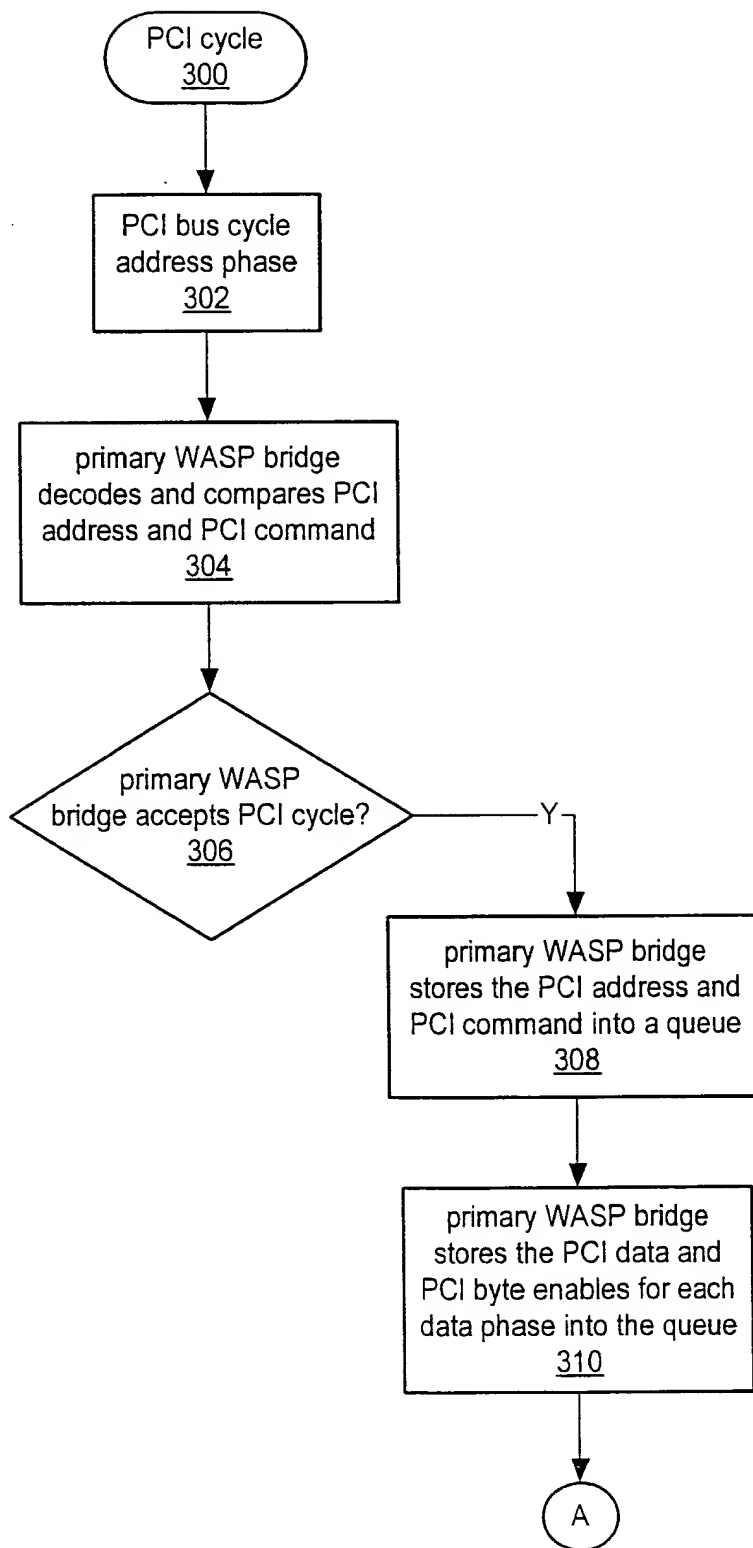


FIG. 11A

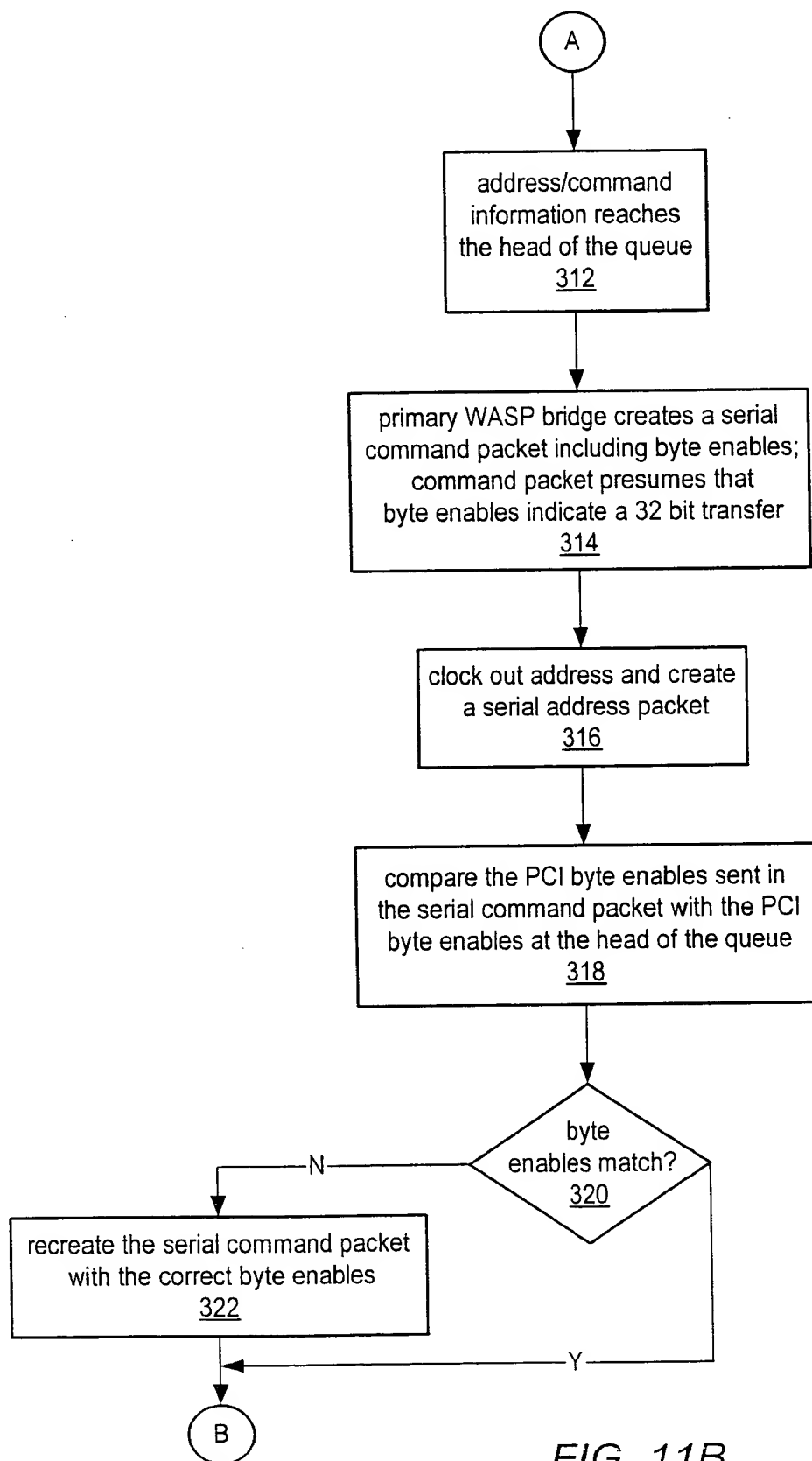
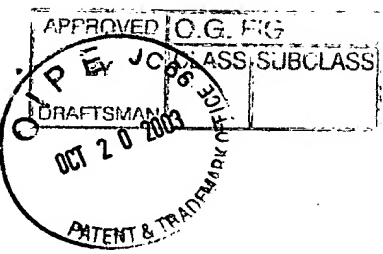


FIG. 11B



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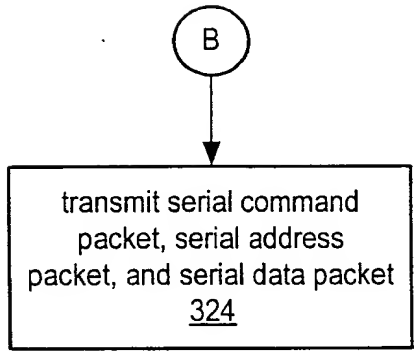


FIG. 11C